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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,988	08/15/2001	Jun Koyama	740756-2348	8058

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EXAMINER	
NGUYEN, CHANH DUY	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 01/29/2004 5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,988	KOYAMA ET AL.	
	Examiner	Art Unit	
	Chanh Nguyen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *7-9,13 and 16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10-12,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/150,933.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species C, Figure 15 directed claims 1-6, 10-12 and 14-15 in Paper No. 4 is acknowledged.

Priority

1. It is noted that this application appears to claim subject matter disclosed in prior Application No. 09/150,933, filed September 10, 1998. A reference to the prior application must be inserted as the first sentence of the specification of this application or in an application data sheet (37 CFR 1.76), if applicant intends to rely on the filing date of the prior application under 35 U.S.C. 119(e) or 120. See 37 CFR 1.78(a). For benefit claims under 35 U.S.C. 120, the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of all nonprovisional applications. Also, the current status of all nonprovisional parent applications referenced should be included.

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/150,933, filed on September 10, 1998.

Information Disclosure Statement

3. The references listed on the Information Disclosure Statement filed on August 15, 2001 have been considered by examiner, see attached PTO-1449.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-6, 10-12 and 14-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,281,865 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other for the reason set forth below.

Claim 1 of application 09/928,988	***Claim 1 of U.S. Patent 6,281,865***
A semiconductor device comprising :	A liquid crystal display device, comprising:
a substrate having at least one driving circuit comprising a plurality of thin film transistors and clock lines for supplying clock signals to the driving circuit,	a first insulating substrate having at least one driving circuit having driver thin film transistors, a plurality of signal lines, a plurality of scan lines, pixel region having pixel thin film transistors, clock lines for supplying clock signals to the driver

	circuit, black matrices covering the pixel thin film transistors, and wiring lines crossing the clock lines or the base portions of the clock lines;
	a second insulating substrate opposite to the first insulating substrate; and
	a liquid crystal held between the first and second insulating substrates
wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors	wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the driving and pixel thin film transistors and, upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the driving and pixel thin film transistors, and

	wherein said wiring lines are made of the same layer as the black matrices.

Note the comparison above, claim 1 of the instant application is broader than claim 1 of the U.S. Patent 6,281,865. Thus, claim 1 of the instant application is not patentably distinct from claim 1 of the U.S. Patent 6,281,865 because number of limitations such as liquid crystal display device, a first substrate, a second substrate, black matrices recited in the U.S. Patent 6,281,865 are deleted from claim1 of this instant application. It would have been obvious to remove liquid crystal display device , first substrate, second substrate and black matrices where the functionality is not needed.

Claim 5 of application 09/928,988	***Claim 1 of U.S. Patent 6,281,865***
A semiconductor device comprising :	A liquid crystal display device, comprising:
a substrate having at least one driving circuit comprising a plurality of thin film transistors, and clock lines for supplying clock signals to the driving circuit, black matrices over the thin film transistors, and wiring lines crossing the clock lines or the base	a first insulating substrate having at least one driving circuit having driver thin film transistors, a plurality of signal lines, a plurality of scan lines, pixel region having pixel thin film transistors, clock lines for supplying clock signals to the driver

portions of the clock lines, wherein said wiring lines comprises the same layer as the black matrices.	circuit, black matrices covering the pixel thin film transistors, and wiring lines crossing the clock lines or the base portions of the clock lines;
	a second insulating substrate opposite to the first insulating substrate; and
	a liquid crystal held between the first and second insulating substrates
	wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the driving and pixel thin film transistors and, upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the driving and pixel thin film transistors, and
wherein said wiring lines comprises the same layer as the black matrices.	wherein said wiring lines are made of the same layer as the black matrices.

Note the comparison above, claim 5 of the instant application is broader than claim 1 of the U.S. Patent 6,281,865. Thus, claim 5 of the instant application is not patentably distinct from claim 1 of the U.S. Patent 6,281,865 for the same reason as discussed above.

Claim 10 of application 09/928,988	***Claim 3 of U.S. Patent 6,281,865***
A semiconductor device comprising:	A liquid crystal display device comprising:
a substrate having at least one driving circuit comprising a plurality of thin film transistors, and clock lines for supplying clock signals to the driving circuit, and at least one shielding line biased at a fixed potential,	a first insulating substrate having at least one driving circuit having driver thin film transistors, a plurality of signal lines, a plurality of scan lines, pixel region having pixel thin film transistors, clock lines for supplying clock signals to the driver circuit, black matrices covering the pixel thin film transistors, and at least one shielding line biased at a fixed potential;
	a second insulating substrate opposite to the first insulating substrate; and
wherein said shielding line is disposed on an interval between the clock lines.	a liquid crystal held between the first and second insulating substrates, wherein said shielding line is disposed on an interval between the clock lines or base portions of the clock lines over the

	first insulating substrate.

Note the comparison above, independent claim 10 of the instant application is broader than claim 3 of the U.S. Patent 6,281,865. Thus, claim 10 of the instant application is not patentably distinct from claim 3 of the U.S. Patent 6,281,865 for the same reason as discussed above.

As to dependent claims 2-4, , 6, 11-12, 14 and 15 , these dependent claims recited the same limitations as dependent claims of the U.S. Patent 6,281,865.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by applicant's admitted prior art (Figures 5 and 6).

Applicant's admitted prior art (Figures 5 and 6) discloses the most closely resembling the subject mater of the claims including thin film transistor, clock lines, two layer structures and black matrices as recited in the claims.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 10-12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art admitted by applicant in view of Watanabe et al (U.S. Patent No. 5,815,223).

As to claim 10, note the discussion of prior art above, prior art admitted by applicant discloses a semiconductor as recited in claim 10 with exception that the prior art does not mention shielding line. Mitra teaches a well-known shielding line (103) disposed on interval between the clock lines (101). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used shielding line as taught by Mitra to the semiconductor of the prior art so as to help prevent clock signals propagated on the clock line from electromagnetically coupling with other signal lines .

As to claims 11-12 and 14-15, the limitations recited in these claims are met by the prior art admitted by applicant (Figures 5-6).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watanabe et al (U.S. Patent No. 5,815,223) and Fukumoto (U.S. Patent No. 5,933,204) are cited to teach well-known feature black matrices and shielding layer.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (703) 308-6603.

If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Steven Saras can be reached at 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

CN

C. Nguyen
January 24, 2004

CHANH NGUYEN
PRIMARY EXAMINER